CLAIMS

What is claimed is:

1. A method of processing, comprising:
forming an impurity region in a device region of a semiconductor-on-insulator substrate, the impurity region defining a junction; and
forming a dislocation region in the device region, the dislocation region traversing the junction.

2. The method of claim 1, wherein the forming of the impurity region comprises forming a source/drain extension region and another impurity region overlapping the source/drain extension region.

3. The method of claim 2, wherein the source/drain extension region and the another impurity region are formed by ion implantation.

4. The method of claim 1, comprising forming a gate electrode on the device region.

5. The method of claim 1, wherein the forming of the dislocation region comprises forming an amorphous region in the device region and heating the semiconductor-on-insulator substrate to recrystallize the amorphous region.

6. The method of claim 5, wherein the forming of the amorphous region comprises implanting a neutral species ions into the device region.

7. A method of processing, comprising:
forming an impurity region in a device region of a substrate, the impurity region defining a junction; and
forming at least two dislocation regions in the device region, the at least two dislocation regions traversing the junction.

8. The method of claim 7, wherein the forming of the impurity region comprises forming a source/drain extension region and another impurity region overlapping the source/drain extension region.

9. The method of claim 8, wherein the source/drain extension region and the another impurity region are formed by ion implantation.

10. The method of claim 8, wherein a first of the at least two dislocation regions traverses a portion of the junction proximate the source/drain extension region and a second of the at least two dislocation regions traverses a portion of the junction proximate the another impurity region.

11. The method of claim 7, comprising forming a gate electrode on the device region.

12. The method of claim 7, wherein the forming of the at least two dislocation regions comprises forming at least two amorphous regions in the device region and heating the semiconductor-on-insulator substrate to recrystallize the at least two amorphous regions.

13. The method of claim 12, wherein the forming of the at least two amorphous regions comprises implanting neutral species ions into the device region.

14. A method of processing, comprising:

forming a first impurity region and a second impurity region in a device region of a semiconductor-on-insulator substrate, the first impurity region defining a first junction and the second impurity region defining a second junction;

forming a first dislocation region in the device region, the first dislocation region traversing the first junction; and

forming a second dislocation region in the device region, the second dislocation region traversing the second junction.

15. The method of claim 14 wherein the forming of the first impurity region comprises forming a first source/drain extension region and a first overlapping impurity region overlapping the source/drain extension region, and the forming of the second impurity region comprises forming a second source/drain extension region and second overlapping impurity region overlapping the second source/drain extension region.

16. The method of claim 15, wherein the first and second source/drain extension regions and the first and second overlapping impurity regions are formed by ion implantation.

17. The method of claim 14, comprising forming a gate electrode on the device region.

18. The method of claim 14 wherein the forming of the first and second dislocation regions comprises forming a first amorphous region and a second amorphous region in the device region and heating the semiconductor-on-insulator substrate to recrystallize the first and second amorphous regions.

19. The method of claim 18, wherein the first dislocation region is formed before the second dislocation region.

20. The method of claim 18, wherein the forming of the first and second amorphous regions comprises implanting neutral species ions into the device region.

21. A circuit device, comprising:
a semiconductor-on-insulator substrate having a device region;
an impurity region in the device region, the impurity region defining a junction; and
a dislocation region in the device region, the dislocation region traversing the junction.

22. The circuit device of claim 21, wherein the impurity region comprises an extension region and an overlapping region.

23. The circuit device of claim 22, wherein the dislocation region traverses the junction proximate the extension region.

24. The circuit device of claim 22, wherein the dislocation region traverses the junction proximate the overlapping region.

25. The circuit device of claim 21, comprising a gate electrode.

26. The circuit device of claim 21, comprising a plurality of dislocation regions traversing the junction.

27. The circuit device of claim 21, wherein the device region comprises silicon.

28. A circuit device, comprising:
a semiconductor-on-insulator substrate having a device region;
a first impurity region in the device region, the first impurity having a first extension region and defining a first junction;
a second impurity region in the device region, the second impurity region having a second extension region and defining a second junction, the second junction being separated from the first junction to define a channel;
a first dislocation region in the device region, the first dislocation region traversing the first junction; and
a second dislocation region in the device region, the second dislocation region traversing the second junction.

29. The circuit device of claim 28, wherein the first dislocation region traverses the first junction proximate the first extension region.

30. The circuit device of claim 29, wherein the second dislocation region traverses the second junction proximate the second extension region.

31. The circuit device of claim 28, comprising a first plurality of dislocation regions traversing the first junction and a second plurality of dislocation regions traversing the second junction.

32. The circuit device of claim 28, comprising a gate electrode.

33. The circuit device of claim 28, wherein the device region comprises silicon.